UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,635	07/23/2001	James A. McCall	42390P11996	3571

8791 7590 12/19/2002

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,635	MCCALL ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 5, 7, 12, 13, 18-20, 22 and 25 are objected to because of the following informalities:

In Claim 5, line 2: "impendence" should be changed to --impedance--.

In Claim 7, line 7: after "chips", the word "for" should be changed to --of--.

In Claim 12, line 2: --connector-- should be inserted after "module".

In Claim 12, line 3: --connector-- should be inserted after "module".

In Claim 13, line 2: --connector-- should be inserted after "module".

In Claim 13, line 3: --connector-- should be inserted after "module".

In Claim 18, line 2: "boards" should be changed to --board--.

In Claim 19, line 1: "module 1" should be changed to --the first module--.

In Claim 19, line 2: "module 2" should be changed to --the second module--.

In Claim 20, line 8: --data-- should be inserted after "first".

In Claim 20, line 8: "with" should be changed to --which--.

In Claim 20, line 13: --data-- should be inserted after "second".

In Claim 20, line 13: "with" should be changed to --which--.

In Claim 22, line 2: --data-- should be inserted after "first" and "second".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 4-6, 10, 21 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 15 recites the limitation "*the first and second chips* of the second module has no antecedent basis (italic/underlined emphasis by the Examiner). Depending on what the Applicant contemplates as the invention, it would seem that, perhaps, this rejection might be overcome if, **either** "*the first module*" were changed to --the second module-- in line 12, **or**, **alternatively**, "*the*" before "first" in line 15 were deleted. What precisely does the Applicant contemplate as the invention of Claim 1?

Claims 4 and 5 recite "R-termination elements." The recitation "R-termination" is an indefinite term since it does not require resistors per se; rather, it can be interpreted as a termination impedance in general involving any types of components. What components does the Applicant contemplate for R-terminations; are R-terminations limited to resistors only? The Examiner will broadly interpret the limitation as a termination impedance formed by any components, including resistors, transistors, etc.

Claim 6 recites the limitation "the second path" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "the third path" and "the fourth path" in line 2. There is insufficient antecedent basis for these limitations in the claim.

Claims 21 and 23 each recite the limitation "the path" in line 2. There is insufficient antecedent basis for this limitation in the claim. Which "path" is

contemplated: the first data path, the second data path, some other path? Furthermore, Claims 21 and 23 both recite identical subject matter and both depend from base Claim 20, so it appears that one of Claims 21 and 23 should be cancelled.

Double Patenting

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 25-29 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of Claims 21, 22, 25, 26 and 29, respectively, of copending Application No. 09/911,760, filed July 23, 2001. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

6. Claims 25-29 are directed to the same invention as that of Claims 21, 22, 25, 26 and 29, respectively, of commonly assigned Application No. 09/911,760. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of

the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

Rejections Based On Prior Art

7. The following references were relied upon for the rejections hereinbelow:

Gay et al. (US 5,467,455)* *Ilkbahar* (US 6,026,456)

Karabatsos (US 6,266,252 B1)* *Osaka et al.* (US 6,438,012 B1)

*Already made of record by Applicant's IDS, Paper No. 5.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Gay et al.

As to Claim 30, Gay et al. discloses a DRAM 10 comprising: a stub 13 to pass bus data from bus 17 to the on-chip elements (col.4: 15-17); an inherent capacitive load due to the various on-chip elements loading on-chip signal lines (i.e., the various on-chip elements including the chip bond pads, the tristate buffer transistors 22, 24, logic gate circuitry 30, 34 and data unit circuitry 18); selectable on die termination 14 coupled to the stub and load (col.5, lines 5-10 and 20-25).

As to Claim 31, Gay et al. further discloses that on die termination 14 includes R-termination (resistor) elements (col.4: 32-34) which may be individually enabled or disabled as per col.5, lines 5-10 and 20-25.

10. Claims 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Osaka et al.

As to Claim 20, Osaka et al. discloses, in Fig. 1: first and second modules 2-2 and 2-3; a circuit board 1 including first and second module connectors d2 and d3 (Fig. 1; col.5: 4-6) receiving first and second modules 2-2 and 2-3, respectively; a first data path of conductors--i.e., the left-to-right data path in Fig. 1 from the memory controller 10-1 to the memory chip modules 2-2 and 2-3 for the memory controller 10-1 to "write" to memory chips 10-2,-3,-4,-5 (col.4: 22-23); this first "write" path is better illustrated in the embodiment of Fig. 4 which is fundamentally based on the Fig. 1 embodiment: col.7: 19-38--, said conductors including lines 1-1 and directional couplers C2 and C3, extending from circuit board 1 to the first module connector d2, to the first module 2-2, back to the first module connector d2, to the circuit board 1, to second module connector d3, to the second module 2-3, and to on module terminations Rtt of second

module 2-3, wherein the first path in first module 2-2 is connected to stubs 1-2 and 1-3 which in turn are coupled to stubs (bumps, balls, leads, traces, etc.) of first and second chips 10-2 and 10-3 of first module 2-2; a second data path of conductors--i.e., the right-to-left data path from the memory chip modules 2-3 and 2-2 to the memory controller 10-1 for the memory controller to "read" from the memory chips 10-2,-3,-4,-5 (col.4: 22-23); better illustrated in the embodiment of Fig. 4 which is fundamentally based on the Fig. 1 embodiment: col.7: 39-62 --, said conductors including lines 1-1 and directional couplers C5 and C4, extending from the circuit board 1 to the second module connector d3, to the second module 2-3, back to the second module connector d3, to the circuit board 1, to the first module connector d2, to the first module 2-2, and to on module terminations Rtt of the first module, wherein the second path in the second module 2-3 is connected to stubs 1-5 and 1-4 which in turn are coupled to stubs (balls, bumps, leads, traces etc.) of first and second chips 10-5 and 10-4 of second module 2-3.

As to Claims 21 and 23 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection, above), Osaka et al. further discloses that there are module connector connections between the circuit board 1 and the first and second module connectors d2 and d3 on the first data path and also on the second data path (Fig. 1).

As to Claim 22, Osaka et al. further discloses additional paths having a path like that of the first and second data paths; e.g., "write" paths from memory controller 10-1 to a chip 10-6 or 10-7 on module 2-4 and "read" paths from a chip 10-6 or 10-7 on module 2-4 to memory controller 10-1.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 2, 4-7, 10-13, 15-17, 19, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilkbahar.

As to Claim 1 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection, above):

I. Ilkbahar discloses, in Fig. 3: first and second modules 322 and 332, respectively; a circuit board 300 including first and second module connectors 320 and 330 to receive the first and second modules 322 and 332, respectively; a first path of conductors extending from bus conductors 305 of the circuit board 300 to the first module connector 320, to the first module 322, back to the first module connector 320, to the circuit board 300, to the second module connector 330 and to the second module 332 (col.6: 14-30); the first path in first module 322 couples to stubs 326 (col.7: 19-20) for first and second chips 324 of first module 322 (in the case wherein first module 322 is a multichip module; see col.4: 15-18) and the first path in the second module 332 couples to stubs 326 for first and second chips 324 of first module 322 (by means of the circuit portion formed by bus 305 on motherboard 300, the contacts of connectors 320 and 330, and the circuitry of modules 322 and 332; see Fig. 3 and col.6: 11-42); each of

the first and second chips 324 include selectable on die terminations (col.6: 31-32 and 35-36; col.7: 46-51; col.8: 60-67).

II. Ilkbahar does not specifically teach that the die terminations of the first and second chips 324 of first module 322 are disabled and the on die terminations of first and second chips 334 of second module 332 are enabled.

III. Ilkbahar teaches that, in general, the termination on the chips of one multichip module, say first module 322, could be disabled while the chips of another multichip module, say second module 332, are enabled in order to enhance the performance of the circuit system comprising the above-cited modules and chips, and for the system to consume less power (col.7: 61-65 and col.8: 49-67).

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the on die terminations of the first and second chips 324 of first module 322 to be disabled and the on die terminations of first and second chips 334 of second module 332 to be enabled in order to enhance the performance of the system with less power consumed by the system, as taught by Ilkbahar.

As to Claim 2, Ilkbahar discloses all the limitations of base Claim 1. However, If the "stubs" in the limitation "...the first path in the first module couples to stubs for first and second chips of the first module" (Claim 1, lines 10-11) are considered to be the balls, bumps, leads, or traces for the first and second chips 324 of first module 322, *instead* of stubs 326, then Ilkbahar clearly teaches the limitation of Claim 2, wherein the first path in the first module 322 is coupled to the stubs (i.e., the aforementioned balls,

bumps, leads or traces) for the first and second chips 324 through *longer* stubs 326 (Fig. 3; col.7: 19-20).

As to Claim 4, Ilkbahar further discloses that each of the on-die terminations include multiple R-termination elements (pull-up and pull-down transistors) which may be individually enabled or disabled (col.7: 52-60; col.8: 49-59).

As to Claim 5, Ilkbahar further discloses that the number of R-termination elements selected in an enabled on die termination is chosen to select a desired impedance (col.8: 35-39).

As to Claims 6 and 10 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection, above) and Claim 7:

I. Ilkbahar discloses that the first and second modules 322 and 332 are multichip modules (col.4: 11-18) with a first path which couples to stubs for chips 324 on first module 332 with selectable on die terminations (Fig. 3; col.7: 19-20; col.8: 35-39 and 49-67) but does not teach additional paths like that of the first path.

II. Since the multichip modules could have any number of chips (including third and fourth chips 334 mounted on second module 332) mounted thereon in any configuration suitable for an application, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have additional paths like that of the first path coupling to stubs for additional chips (including third and fourth chips 334 of second module 332) with selectable on die terminations (col.6: 31-32 and 35-36; col.7: 46-51; col.8: 60-67) including the case wherein the third and fourth chips 334 of second module 332 are disabled and the on die terminations of third and fourth chips of first

module 322 are enabled in order to increase the functionality or memory capacity of the system as well as enhancing system performance while reducing system power consumption (col.7: 61-65 and col.8: 49-67).

As to Claim 7:

I. Ilkbahar does not teach the claimed second path, third and fourth chips on each of the first and second modules, stubs for the third and fourth chips, selectable on die terminations on each of the third and fourth chips of the first and second modules, and wherein the third and fourth chips of the second module are disabled and the terminations of the third and fourth chips of the first module are enabled.

II. Ilkbahar teaches that, plural chips 324 and plural chips 334 on the first and second modules 322 and 332, i.e., multichip modules (col.4: 15-18), and further teaches that, in general, the termination on the chips of one multichip module, say first module 322, could be disabled while the chips of another multichip module, say second module 332, are enabled in order to enhance the performance of the circuit system comprising the above-cited modules and chips, and for the system to consume less power (col.7: 61-65 and col.8: 49-67).

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to establish a second path for third chips and fourth chips 324 and third and fourth chips 334 on each of the first and second modules that couple to stubs of the third and fourth chips on each of the first and second modules, analogous to the electrical structure including the first path, stubs and the first and second chips of base Claim 1 (see rejection of base Claim 1, above), and furthermore to

enable the on die terminations of the third and fourth chips 334 of second module 332 to be disabled and the on die terminations of third and fourth chips 324 of first module 322 to be enabled in order to enhance the performance of the system with less power consumed by the system, as taught by Ilkbahar.

As to Claim 11, Ilkbahar further discloses a controller 310 coupled to the first and second paths (col.6: 15-17 and 35-36).

As to Claim 12, Ilkbahar further discloses, in Fig. 3, that first and second module connectors 320 and 330 (col.6: 17-20) each have (in the direction from left to right in Fig. 3) front sides and back sides, and the first path extends from the back side of the first module connector 320 to the back side of the second module connector 330.

As to Claim 13, Ilkbahar further discloses, in Fig. 3, that first and second module connectors 320 and 330 (col.6: 17-20) each have (in the direction from left to right in Fig. 3) front sides and back sides, and the first path extends from the back side of the first module connector 320 to the front side of the second module connector 330.

As to Claims 15 and 16:

I. Ilkbahar discloses that modules 322 and 332 can be multichip modules, memory modules, etc. (col.4: 15-18) but does not teach the specific circuitry and components mounted thereon, including buffers and error correction code chips, for an application.

II. Buffers and error correction code chips are old and well-known devices for performing specific functions in an electronic circuit mounted on a modular or system circuit board. Buffers have various electronic circuit functions: *inter alia*, as storage

sites that temporarily store data during data transfers to compensate for differences in data flow rates. Error correction code (ECC) chips are typically used for generating correction code when data is written into a memory chip and for checking "read" data to correct errors when data is read from the memory chip.

III. Since Ilkbahar discloses multichip modules including memory devices, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to use buffers and ECC chips on the modules 322 and 332 of Ilkbahar in order to enable the disclosed electronic system by managing the data flow between the modules and the memory chips thereon.

As to Claim 17, Ilkbahar further discloses that circuit board 300 is a printed circuit board and a motherboard (col.6: 21-30).

As to Claims 1 and 19:

A) In Claim 1 (as best understood by the Examiner in view of the 35 USC § 112, 2nd paragraph rejection of Claim 1, above):

I. Ilkbahar discloses, in Fig. 3: first and second modules 322 and 342, respectively; a circuit board 300 including first and second module connectors 320 and 340 to receive the first and second modules 322 and 342, respectively; a first path of conductors extending from bus conductors 305 of the circuit board 300 to the first module connector 320, to the first module 322, back to the first module connector 320, to the circuit board 300, to the second module connector 340 and to the second module 342 (col.6: 14-30); the first path in first module 322 couples to stubs 326 (col.7: 19-20) for first and second chips 324 of first

module 322 (in the case wherein first module 322 is a multichip module; see col.4: 15-18) and the first path in the second module 342 couples to stubs 326 for first and second chips 324 of first module 322 (by means of the circuit portion formed by bus 305 on motherboard 300, the contacts of connectors 320, 330 and 340, and the circuitry of modules 322, 332 and 342; see Fig. 3 and col.6: 11-42); each of the first and second chips 324 include selectable on die terminations (col.6: 31-32 and 35-36; col.7: 46-51; col.8: 60-67).

II. Ilkbahar does not specifically teach that the die terminations of the first and second chips 324 of first module 322 are disabled and the on die terminations of first and second chips 344 of second module 342 are enabled.

III. Ilkbahar teaches that, in general, the termination on the chips of one multichip module, say, the first module 322, could be disabled while the chips of another multichip module, say, the second module 342, are enabled in order to enhance the performance of the circuit system comprising the above-cited modules and chips, and for the system to consume less power (col.7: 61-65 and col.8: 49-67).

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made enable the on die terminations of the first and second chips 324 of first module 322 to be disabled and the on die terminations of first and second chips 344 of second module 342 to be enabled in order to enhance the performance of the system with less power consumed by the system, as taught by Ilkbahar.

B) In Claim 19, Ilkbahar further discloses an additional module 332 between first module 322 and second module 342 (Fig. 3).

As to Claim 30:

I. Ilkbahar discloses: modules having plural chips 324 thereon including memory chips (Fig. 3; col.4: 15-18); a stub to pass data (col.7: 19-20), i.e., a portion of the on chip circuitry, such as a ball, bump, lead, trace, etc.; an inherent capacitive load due to the various on-chip elements loading on-chip signal lines (e.g., the various on-chip elements including the chip bond pads, transistors, logic gate circuitry, memory and data unit circuitry); and selectable on die terminations coupled to the stub and load (col.8: 35-39 and 60-67).

II. DRAMs (Dynamic Random Access Memory) are old and well-known memory chips widely used in the art of memory modules (e.g., SIMMs and DIMMs) since they are small and relatively inexpensive. Therefore, it would have been obvious to populate the memory modules of Ilkbahar with DRAMs in order to provide the main or add-on memory for the electronic system disclosed in Fig. 3 of Ilkbahar.

As to Claim 31, Ilkbahar further discloses that the on die termination includes multiple R-termination elements which may be individually enabled or disabled (col.7: 52-53; col.8: 35-39 and 49-67).

13. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Osaka et al. in view of Karabatsos.

I. Osaka et al. does not disclose that first and second module connectors d2 and d3 are keyed such that a similarly keyed module 2-2 or 2-3 can be inserted in only one orientation into the corresponding module slot in each of connectors d2 and d3.

II. Karabatsos discloses modules 10, 12, 14 mounted in slots of connectors 8 wherein the connectors 8 and modules 10, 12, 14 are keyed (note the notches separating portions of finger contacts 5 on module 10; Fig. 1) so that modules 10, 12, 14 can each be inserted in only one orientation into the corresponding module connector slot in order to ensure proper electrical connection of the modules to the connectors on motherboard 28.

III. Since both Osaka et al. and Karabatsos mount multichip memory modules to a motherboard, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the modules and connectors of Osaka et al. with the keying structures taught by Karabatsos so that the modules of Osaka et al. can each be inserted in only one orientation into the corresponding module connector slot in order to ensure proper electrical connection of the modules to the connectors on the motherboard 1 in Osaka et al., as taught by Karabatsos.

Allowable Subject Matter

14. Claims 3, 8, 9, 14, 18 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. 112, second paragraph, and/or objections set forth in this Office action.

15. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 3, patentability resides in the limitation wherein *the first path in the first module includes a short loop through section and the first path in the second module does not include a short loop through section*, in combination with the other limitations of the claim.

As to Claim 8, patentability resides in the limitation wherein *the first path in the first module is coupled to the stubs for the third and fourth chips through longer stubs*, in combination with the other limitations of the claim.

As to Claim 9, patentability resides in the limitation wherein *the first path in the first module includes a short loop through section and the first path in the second module does not include a short loop through section*, in combination with the other limitations of the claim.

As to Claim 14, patentability resides in the limitation wherein *each of the X paths couples to stubs for a different two of the 2X chips of the first module and for a different two of the 2X chips of the second module*, in combination with the other limitations of the claim.

As to Claim 18, patentability resides in the limitation wherein *impedances of the paths in the first module are at least 50% higher than the paths on the circuit board*, in combination with the other limitations of the claim.

As to Claims 25-29 (subject to the Statutory Double Patenting rejection, above), patentability resides in the limitation wherein *a first section of the second path, which is*

a short loop through section, couples to stubs for third and fourth chips of the second module and a section of the second path couples to stubs for third and fourth chips of the first module, in combination with the other limitations of base Claim 25.

16. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Perino et al. (US 6,067,594) discloses that "a stub is defined as a length of line tapped from a transmission line and having a round trip delay which is greater than the rise time (or fall time) of the signal" (col.2: 5-8). Perino et al. also teaches a keyed module and corresponding keyed connector (Fig. 5; col.5: 14-17 and 58-65).

Osaka et al. (US 5,638,402) discloses a stub as a portion of the bus connecting line 1-2 from an end (or a bending point) of the parallel coupling portion P to the semiconductor integrated circuit 10-2, provided for transferring a signal thereto (Fig. 1; col.5: 26-31).

Haba et al. (US 6,376,904 B1) discloses that "when electrically coupling IC die to signal bussing, the signal lines become loaded with the inherent load capacitance which is due to the various elements of the I/O structures disposed on the integrated circuit,

for example, bond pads, electrostatic discharge protection devices, input buffer transistors, and output driver transistors" (col.2: 3-9).

La Rue (US 6,081,430) discloses controlled impedance lines 13 that are called "loop-through" because "the transmission line starts on the mother board, connects to a transmission line on the daughter board and then connects back to the mother board" (col.3: 35-41). La Rue further discloses stubs 21 between the lines 13 and transceivers 7 (Fig. 4; col.3: 50-52).

Gasbarro (US 6,308,232 B1) discloses, in Fig. 4, memory modules 30 (including B1, B2...BN; col.6: 4-6) connected to connector slots (col.6: 12-19), each memory module having memory devices D_1, D_2,.....D_N. Each module BN has an active terminator 31 thereon (col.6: 6-8). Also disclosed, in Fig. 3, is a plurality of memory devices 20 (including D_1, D_2,.....D_N), each memory device incorporating an active terminator 21 on the device (col.5: 21-25). The active terminators 21 and 31 are selectively enabled/disabled (col.5: 46-51; col.6: 20-34). The active terminators 21 and 31 may be implemented in the form of a transistor switch and a resistor, or just a transistor switch, and may optionally include a coupling capacitor between terminal voltage V_T and the transistor switch (Figs. 6A,B; col.6: 36-48).

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
December 13, 2002